

The rejection of claims 1, 2, 4, 6, 8, 9, 11, and 20 under 35 U.S.C. § 102(e) as being anticipated by Shin is traversed and reconsideration is respectfully requested.

Independent claim 1 is allowable over the cited art in that claim 1 recites a combination of elements including, for example, “a timing controller... for receiving a data clock inputted from the exterior thereof to output the data from the plurality of groups of said line memory to the driving circuit every period of the data clock:...” None of the cited references including Shin, singly or in combination, teaches or suggest at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that independent claim 1 and claims 2-7 and 12, which depend therefrom are allowable over the cited references.

Independent claim 8 is allowable over the cited art in that claim 8 recites a combination of elements including, for example, “a timing controller... for outputting the data in each of the groups to the driving circuit during each period of the first data clock.” None of the cited references including Shin, singly or in combination, teaches or suggest at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that independent claim 8 and claims 9-11, which depend therefrom are allowable over the cited references.

Independent claim 20 is allowable over the cited art in that claim 20 recites a combination of elements including, for example, “a data outputting step of outputting a desired data unit from each of said groups at a different time during one period of the second data clock.” None of the cited references including Shin, singly or in combination, teaches or suggest at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that independent claim 20 and claim 21, which depends therefrom are allowable over the cited references.

The Examiner cites Shin as teaching "...a timing controller (220), being connected to the line memory (230) and the driving circuit (270), for receiving a data clock inputted from the exterior thereof to output the data from the plurality of groups of the line memory (230) to the driving circuit (270) every period of the data clock...(see column 5, line 18-column 6, line 18)." (Office Action at 2, page 3). In the "Response to Arguments" section of the Office Action, the Examiner alleges "Shin clearly teaches in Fig. 8, data from the plurality of groups is outputted every period of the data clock CK2, rather than every other period as argued by the [Applicants]. The timing controller receives a clock signal CK2 from the exterior thereof from the clock generator (200). The clock generator (200) having an input terminal for receiving a first clock signal CK1 and an output terminal for outputting a second clock signal CK2 (see column 5, lines 28-32). Hence, data is output from the plurality of groups of the line memory (230) to the driving every period of the data clock signal CK2 (see column 5, line 65-column 6, line 2)." (Office Action at page 7).

Contrary to Examiner's assertion in the "Response to Arguments" section, Shin does not teach or suggest any timing controller that receives a clock signal CK2 from the exterior thereof from the clock generator 200. Further, Applicants respectfully submit Shin does not disclose a timing controller outputting data every period of a received data clock.

For example, Applicants respectfully submit at column 5, lines 28-32, Shin teaches "driving circuit... includes a clock generator 200 having an input terminal for receiving a first clock signal CK1 and an output terminal for outputting a second clock signal CK2." Further, from column 5, line 56 to column 6, line 18 (with reference to Figure 8) Shin teaches "...a first clock signal is applied. Then, the clock generator 200 produces the second clock signal CK2, the period of which is twice that of the first clock signal CK1: i.e., the clock speed of

the second clock signal CK2 is half that of the first clock signal CK1. According to the first clock signal CK1, the first odd data (video signal)d1 is stored in the odd memory 230a and the first even data (video signal)d2 is stored in the even memory 230b. According to the second clock signal CK2, the first odd data d1 and the first even data d2 are sent to the first odd data driver IC 240 and the first even data driver IC 250, respectively. At that time, the second odd data d3 is stored to the odd memory 230a, and the second even data d4 is stored to the even memory 230b according to the first clock signal CK1. The output of the first pair of data (d1 and d2) and the input of the second pair of data (d3 and d4) are performed at the same time. ...After the line data on the one-page data are latched at all the data driver ICs, all the latched data are sent to the data lines at one time". Referring to Figure 7 of Shin, the first clock signal CK1 is received by the clock generator 200. Referring to Figure 8 of Shin, the "data from the plurality of groups" is not outputted every period of the first clock signal CK1. Rather, the "data from the plurality of groups" is outputted every other period of the first data clock CK1.

The rejection of claims 3, 5, 7, 10, 12-19, and 21 under 35 U.S.C. § 103(a) as being unpatentable over Park et al. in view of Park is traversed and reconsideration is respectfully requested.

Applicants respectfully submit claims 3, 5, 7, 10, 12-19, and 21 are allowable over the cited references in that Park et al. is not prior art under 35 U.S.C. § 103(c). In particular, the present Application was filed after November 29, 1999. The present Application (i.e., Application Serial No. 09/655,937) and Park et al. were, at the time the invention of Application Serial No. 09/655,937 was made, at least owned by and/or subject to an obligation of assignment to the same organization. Therefore, Applicants request withdrawal

of the rejection of claims 3, 5, 7, 10, and 12-19 under 35 U.S.C. § 103(a) as being unpatentable over Park et al. in view of Park.


Applicants believe the application in condition for allowance and early, favorable action is respectfully solicited. Should the Examiner deem that a telephone conference would further the prosecution of this application, the Examiner is invited to call the undersigned attorney at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136. Please credit any overpayment to deposit Account No. 50-0911.

Respectfully submitted,

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